

AUG 31 2001

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,812,530 B2
DATED : November 2, 2004
INVENTOR(S) : Schuegraf et al.

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title Page, **References Cited**, FOREIGN PATENT DOCUMENTS, please insert --JP 401276761-A 11/1989-- before "JP 02265248 A 4/1989".

Title Page 2, **References Cited**, Col. 2, OTHER PUBLICATIONS, please insert --Wolf et al., "Silicon Processing for the VLSI Era - Volume 1: Process Technology," ©1986 Lattice Press, pages 384-385 (4 pages total)-- after "Lee, B. et al." reference.

Col. 6, line 26, claim 11, please delete "suicide" after "comprising" and insert --silicide--.

Col. 6, line 62, claim 17, please delete "suicide" after "comprising" and insert --silicide--.

Page
1 of 1

Mailing Address of Sender:
D. Brent Kenady
Wells St. John P.S.
601 West First Avenue, Suite 1300
Spokane, WA 99201-3828

Patent No. 6,812,530 B2

AUG 31 2005

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,812,530 B2
DATED : November 2, 2004
INVENTOR(S) : Schuegraf et al.

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title Page, **References Cited**, FOREIGN PATENT DOCUMENTS, please insert --JP 401276761-A 11/1989-- before "JP 02265248 A 4/1989".

Title Page 2, **References Cited**, Col. 2, OTHER PUBLICATIONS, please insert --Wolf et al., "Silicon Processing for the VLSI Era - Volume 1: Process Technology," ©1986 Lattice Press, pages 384-385 (4 pages total)-- after "Lee, B. et al." reference.

Col. 6, line 26, claim 11, please delete "suicide" after "comprising" and insert --silicide--.

Col. 6, line 62, claim 17, please delete "suicide" after "comprising" and insert --silicide--.

Page
1 of 1

Mailing Address of Sender:
D. Brent Kenady
Wells St. John P.S.
601 West First Avenue, Suite 1300
Spokane, WA 99201-3828

Patent No. 6,812,530 B2

AUG 31 2005



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent No. 6,812,530 B2
Patent Issue Date November 2, 2004
Application Serial No. 09/875,501
Filing Date June 4, 2001
Assignee Micron Technology, Inc.
Inventorship Klaus Florian Schuegraf et al.
Attorney's Docket No. MI22-1741
Title: Methods for Forming Wordlines, Transistor Gates, and Conductive
Interconnects, and Wordline, Transistor Gate, and Conductive Interconnect
Structures

**REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT
FOR PTO MISTAKE (37 C.F.R. 1.322(a))**

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
ATTN: Decision and Certificate of Correction
Branch of the Patent Issue Division

From: D. Brent Kenady (Tel. 509-624-4276; Fax 509-838-3424)
Wells St. John P.S.
601 W. First Avenue, Suite 1300
Spokane, WA 99201-3828

Sir:

It is hereby requested that a Certificate of Correction be issued with respect to Patent No. 6,812,530 B2, granted November 2, 2004, in accordance with the Certificate of Correction form attached hereto in duplicate.

The errors listed on the Certificate of Correction form were apparently incurred through the fault of the PTO as will be disclosed by the records of files in the Office.


Since this Certificate of Correction is being requested due to PTO errors, it is believed that no fee is due. However, in the event that a fee is required for issuance of this Certificate of Correction, please charge the fee specified under

37 C.F.R. § 1.20(a) to Deposit Account No. 23-0925. Please credit Deposit Account No. 23-0925 with any overpayment of the above fee.

Attached hereto, in duplicate is Form PTO-1050, with at least one copy being suitable for printing.

Respectfully submitted,

Dated: 8-22-05

By: 
D. Brent Kenady
Reg. No. 40,045